CLAIMS

1. A TFT array substrate comprising;

a plurality of gate lines 2 formed on an insulative substrate 1, each of the gate lines includes a gate electrode,

a plurality of source lines 3 crossing the gate lines, each of the source lines includes a source electrode 7,

a semiconductor layer 5 formed on the gate electrode with a gate insulating film 4 interposed in between,

a thin-film transistor formed by the source electrode 7 and a drain electrode, the source electrode and the drain electrode are connected to the semiconductor layer, and

a pixel electrode 8 connected to a drain line 6 extending from the drain electrode 6,

characterized in that;

the width of a crossing portion of the semiconductor layer 5 and the width of a crossing portion of the drain line 6a overlapping with the semiconductor layer that cross an edge line of the gate electrode 2 are made smaller than the width of the drain electrode that is equal to a channel width 11 of the thin-film transistor.

2. The TFT array substrate according to claim 1, characterized in that the drain electrode 6 and the drain line 6a have portions that are located over the gate electrode 2 and do not coextend with the semiconductor layer 5.

3.A TFT array substrate comprising;

a plurality of gate lines 2 formed on an insulative substrate 1, each of the gate lines includes a gate electrodes,

a plurality of source lines 3 crossing the gate lines, each of the source lines includes a source electrodes 7,

a semiconductor layer 5 formed on the gate electrode with a gate insulating film 4 interposed in between,

a thin-film transistor formed by the source electrode 7 and a drain electrode 6, the source electrode and the drain electrode are connected to the semiconductor layer, and

a pixel electrode having a pixel line 8a connected to the drain electrode 6,

characterized in that;

the width of a crossing portion of the semiconductor layer 5 and the width of a crossing portion of the pixel line 8a overlapping with the semiconductor layer that cross an edge line of the gate electrode 2 are made smaller than the width of the drain electrode 6 that is equal to a channel width 11 of the thin-film transistor.

4. The TFT array substrate according to claim 3, characterized in that said the electrode 6 and the pixel line 8a have portions that are located over the gate electrode 2 and do not coextend with the semiconductor layer 5.

5. A TFT array substrate comprising;

a plurality of gate lines 2 formed on an insulative substrate 1, each of the gate lines includes a gate electrode,

a plurality of source lines 3 crossing the gate lines, each of the source lines includes a source electrodes 7,

a semiconductor layer 5 formed on the gate electrodes 2 with a gate insulating film 4 interposed in between,

a thin-film transistor formed by the source electrode 7 and a drain electrode 6, the source electrode and the drain electrode are connected to the semiconductor layer, and

a pixel electrode 8 having a pixel line 8a connected to the drain electrode 6,

characterized in that;

the width of a crossing portion of the pixel line 8a that crosses an end line of the gate electrode 2 is made smaller than the width of the drain electrode that is equal to a channel width 11 of the thin-film transistor.

6. The TFT array substrate according to claim 5, characterized in that the drain electrode 6 has a portion that is located over the gate electrode 2 and does not coextend with the semiconductor layer 5.

7. A liquid crystal display device characterized in that a liquid crystal is interposed between the TFT array substrate according to any one of claim 1 to 6 and a counter electrode substrate having a transparent electrode, color filters, etc. or a counter electrode substrate having a transparent electrode.